Three-Channel Integrating Analog-to-Digital Converter

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A three-channel integrating analog-to-digital converter has been added to the complex mixer system. It accepts the baseband, complex signals generated by the complex mixers and outputs binary data to the digital demodulator for further processing and recording. It was first used for processing multistation data in radar experiments in the spring of 1977.

I. Introduction

A three-channel integrating analog-to-digital converter (IADC) has been added to the Complex Mixer System (Ref. 1) in the pedestal room at DSS 14. The IADC performs the integrate and dump function, accepting the real and imaginary baseband signals generated by the complex mixers, and supplying six-bit binary integral values to the digital demodulator (DDM) for further processing and recording.

This unit was designed to be operated with the modified complex mixer modules (Ref. 2). Signals from one, two, or three complex mixer modules can be processed simultaneously by the IADC, with each channel receiving its own timing reference signal from the DDM. Integration times of 1.3, 5, 15, or 45 μs can be accommodated by the unit.

II. Equipment Description

A block diagram showing one channel of the three channel IADC is shown in Fig. 1. Three identical but independent complex channels exist within the unit. Each channel is comprised of two identical signal paths whose sampling, conversion, and digital functions are synchronously controlled by a shared timing generator.

The analog signals processed by the IADC are generated by the complex mixers. Real and imaginary baseband signals are produced in each complex mixer module by splitting the IF signal into two paths and mixing with local oscillator signals that are in phase quadrature. The resulting real and imaginary baseband signals are then bandlimited to 2 MHz by low-pass filters and amplified to a nominal output level of 2 V_{p-p}.

Each of the three complex channels within the IADC receives a separate clock signal generated within the DDM. The positive-going transition of each clock pulse initiates a timing sequence within each channel. Timing signals are generated to operate the sampling and conversion processes as well as controlling the digital dump, front panel indicators and output data registers.

Each signal path within this equipment employs a digital dump which calculates an approximation to the desired integral values. This technique is described in detail in Ref. 3. Each analog input signal is first passed through a simple RC low-pass filter which acts as an imperfect integrator. The filtered signal is then amplified, sampled, and A-D converted. The digital sample values are then fed to data registers contained within the digital dump logic. One register holds the current sample value, while a second register holds the previous sample value.

From these two values, the digital dump calculates an approximation to the required integral ΔE from

$$\Delta E = E_n - \frac{3}{4} E_{n-1}$$

where E_n is the present voltage sample, and E_{n-1} is the previous voltage sample.

The low-pass filter time constant τ is determined by the word size in the dump logic and the integration time T. The ratio T/τ is chosen to minimize errors introduced by this technique. For this equipment

$$\frac{T}{\tau} = 0.288$$

with a corresponding degradation of less than 0.1 dB when compared to a perfect integrate and dump. This unit has been operated at various sampling rates from 1.3 to 45 μs by selecting appropriate filter time constants and associated gain control elements.

The internal sample values and the computed integral values are bipolar 8-bit numbers. The word size of the output data is 6-bits, with negative values represented in two's complement. Front panel data/ $\overline{\text{data}}$ switches allow the selection of positive-true or one's-complemented output data. A front panel gain control switch associated with each complex channel allows the user to select the desired binary scaling of the 6-bit data word.

Three positions are available:

X1: In this mode, the sign bit (bit 1) and the five adjacent bits (2 through 6) of the 8-bit integral value are selected as the output data word. No overflows can occur in this mode. Rounding is provided in this gain position.

X2: In this mode, the sign bit plus the five intermediate bits (3 through 7) of the 8-bit integral value are selected. In this mode, the full-scale integral values that can be represented in the 6-bit data word is reduced to one-half of that that could be represented in the X1 gain mode. Simultaneously, the resolution is increased by a factor of two by using these lower order bits. Should a rollover occur into the unused bit 2, the condition is detected, and the appropriate positive or negative full-scale code is forced onto the output data lines. A front panel light-emitting diode (LED) indicator is simultaneously pulsed on, indicating that the saturation has occurred. Rounding is provided in this gain position.

X4: In this mode, the sign bit and the five least significant bits (4 through 8) of the computed integral value are selected. Rollovers are detected, corrected and displayed.

When operating in the X2 or X4 gain modes, internal overflows can occur. These overflows are detected, and the output data lines are forced to the appropriate saturation code. In addition, the occurrence of an overflow in one of the channels triggers a one-shot multivibrator and driver which momentarily turns on a front panel LED indicator, yielding a visual indication that the data saturation has occurred. Each of the six signal channels has two associated LEDs, one for positive and one for negative data saturations. Occasional flashing of these indicators indicates that the full dynamic range of the IADC is being exercised. Continuous illumination of any LED indicates improper signal level adjustment or hardware failure.

The analog signals supplied to the IADC should have a level of approximately 0.33 V_{rms}. At this level, 3 σ noise peaks of 2 V_{p-p} will be passed without clipping. Six input signal level monitors continuously check the input signal levels and drive front panel meters. These monitors are not intended for use in making precise measurements, as these simple uncalibrated meters are used only to confirm proper input signal levels. A red line on each meter face indicates the nominal reading.

III. Performance

The IADC is designed to process the baseband output signals generated by the complex mixers and supply output data to the DDM. Input and output characteristics were therefore determined by these systems. Table 1 summarizes the IADC's specifications.

IV. Packaging

The three-channel IADC is a self-contained rack-mounted unit that occupies 17.8 cm (7 in.) of rack space. Four wire wrap boards hold the digital logic and A-D converter modules. These four logic boards plus power supplies are mounted within the logic cage pictured in Fig. 2. Figure 3 shows the component side of one of the logic boards.

V. Summary

A three-channel IADC has been added to the complex mixer system. Installed in the pedestal room at DSS 14 in March of 1977, this unit was used to process planetary radar signals received at DSS 12, DSS 13 and DSS 14 in March and April.

References

1. Constenla, L. C., *Complex Mixer System,* Technical Report 32-1526, Jet Propulsion Laboratory, Pasadena, California, Dec. 15, 1972.

2. Stevens, G. L., "Complex Mixer System Modifications," in *The Deep Space Network Progress Report 42-42,* Jet Propulsion Laboratory, Pasadena, California, Dec. 1977.

3. Winkelstein, R. A., "High Rate Telemetry Project, Digital Equipment," in *The Deep Space Network,* Space Programs Summary 37-48, Vol. II, pp. 111-112, Jet Propulsion Laboratory Pasadena, California, Nov. 30, 1967.

Table 1. Three-channel IADC specifications

Parameter	Value	Comment
Sampling period	1.3,5,15 or 45μs	
Input impedance	50 Ω	Each of 6 analog inputs
Input signal level	0.33 V_{rms}	Nominal output level of complex mixers
Input signal bandwidth	DC to 2 MHZ	Nominal bandwidth of complex mixers
Output word size	6 bits	
Output coding	2's complement	Negative values are represented in 2's complement
Output polarity	Positive-true or one's complemented	Controlled by front panel DATA/$\overline{\text{DATA}}$ switches

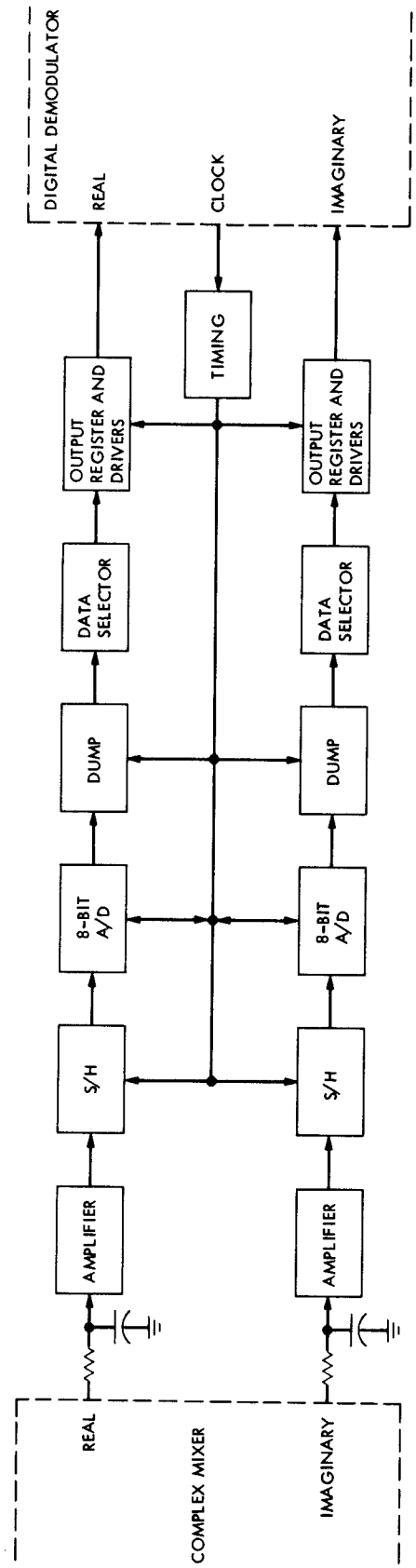

Fig. 1. Block diagram showing one channel of the three-channel IADC

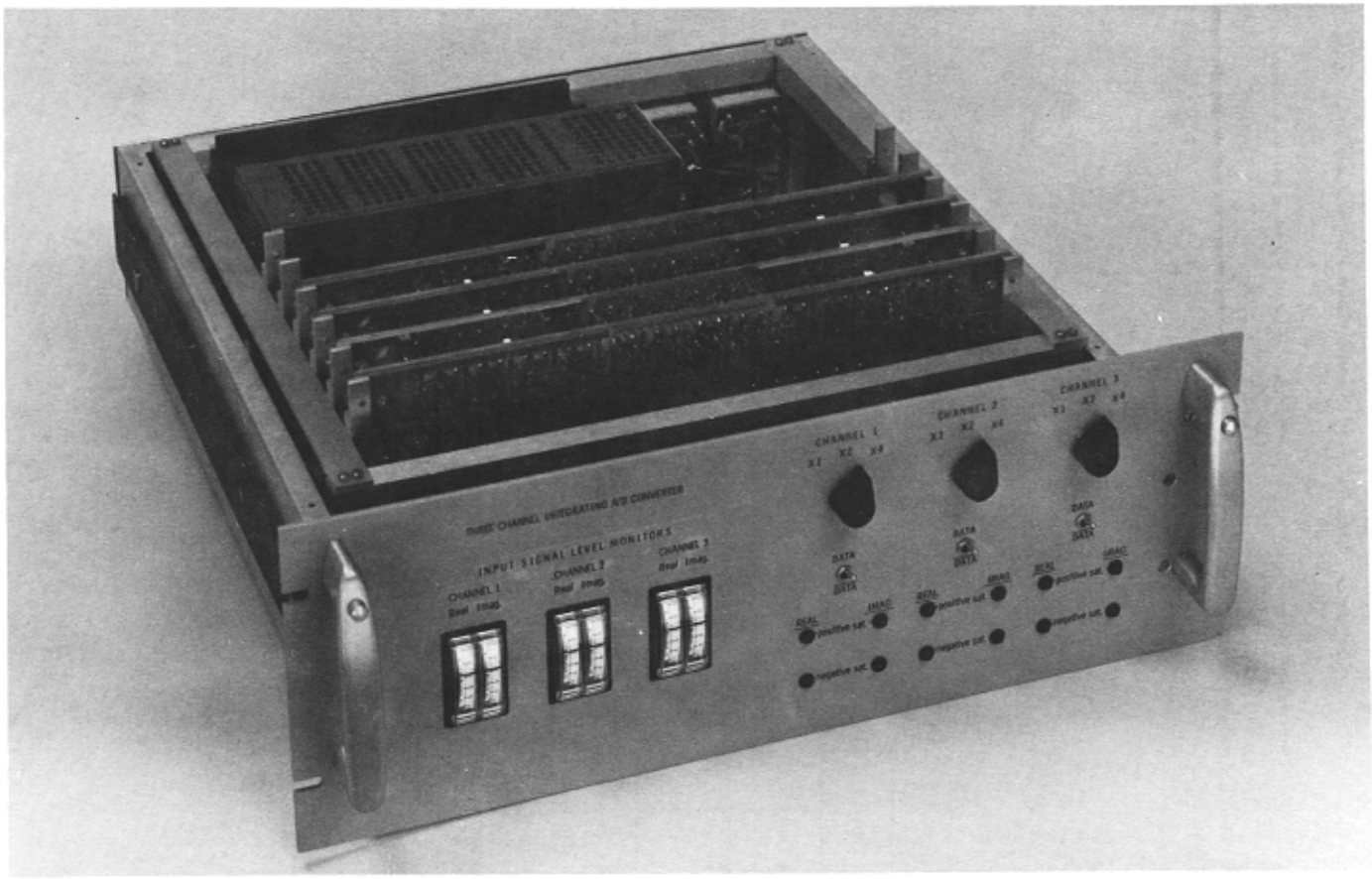

Fig. 2. Three-channel integrating analog-to-digital converter

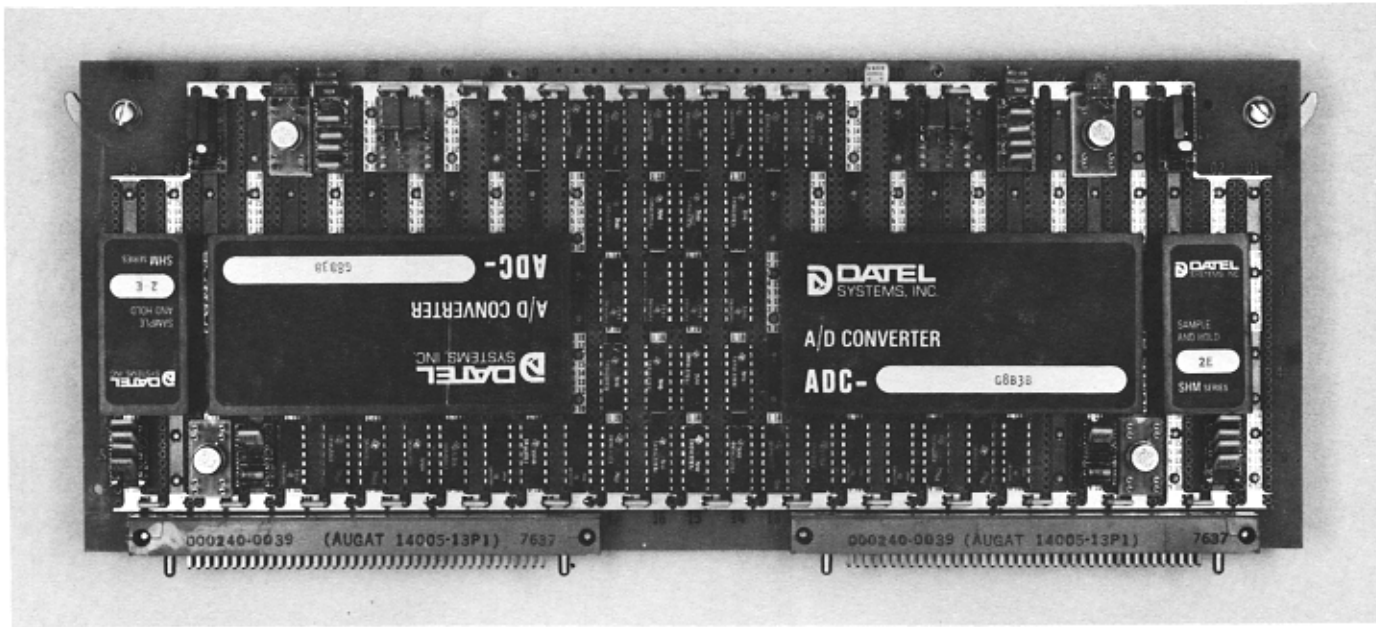

Fig. 3. Component side of analog-to-digital converter card